Total No. of Printed Pages:2

SUBJECT CODE NO:- P-100
FACULTY OF ENGINEERING AND TECHNOLOGY
S.E.(CSE/IT) Examination MAY/JUNE-2016
Digital Electronics
(Revised)

[Time:Three Hours] **[Max Marks:80]**

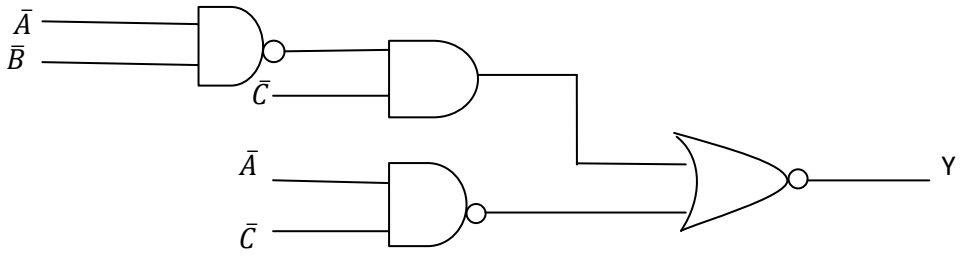
"Please check whether you have got the right question paper."

N.B i) Q.No.1 from section A and Q.No.6 from section B are compulsory, solve any two questions from remaining, from each section.
ii) Figures to the right indicate full marks.
iii) Assume suitable data, wherever necessary.

Section A

Q.1 Solve **any five** 10

a) Design Boolean expression of y for the given logic diagram



b) Reduce following using Boolean algebra
Y=F(A,B,C)=$\sum m\ (0,1,3,5)$

c) Construct truth table for 4-input AND gate.

d) Draw 4-variable K-map.

e) What is PAL.

f) Convert following SOP expression to POS form
F=$\sum m(0,1,5,6,8,9,11,13) + \sum d(7,10,12)$

g) Draw the logic symbol of clocked JK-FF write its truth table.

h) Explain encoder with example.

Q.2 a) Minimize the following using Quine Mc-cluskey method 08
F=πN(1,2,3,8,9,10,11,14) .$\pi D(7,15)$

b) Design 2-bit digital comparator. 07

Q.3 a) What is digital signal? Explain different characteristics of digital signal. 07

b) Implement following Boolean expression using BCD to decimal decoder & NAND gates only 08

i) F=$\sum m(0,2,3,5,7)$

ii) F=$\sum m(1,3,4,6,7)$

iii) F=$\sum m(0,2,4,5,6,7)$

Q.4 a) Design 10 bit even parity generator. 08
b) Compare combinational & sequential circuits. 07

Q.5 a) Design a combinational logic circuit that accepts a 4-bit binary number & output is 1 , it is an even number 07
b) Design 16:1 MUX using 4:1 multiplexer only Explain its working. 08

Section B

Q.6 Solve **any Five** 10

a) Enlist types of shift register.
b) Draw & explain NAND implementation of 1-bit memory cell
c) Draw logic diagram for 4-bit SISO register.
d) What is counter?
e) How many flip-flops are needed to design following counter?
   1) MOD-16
   2) MOD-10
f) Draw block diagram of DAC.
g) Write applications of ADC.
h) Draw the diagram of left shift register.

Q.7 a) Explain working of universal shift register IC 7495 07
b) Explain binary weighted register D to A convertor 08

Q.8 a) Design synchronous decode counter using T-type flip-flop 08
b) Explain working of dual / slope ADC. 07

Q.9 a) Compare synchronous and Asynchronous counter. 08
b) Explain PIPO shift register IC 74198. 07

Q.10 a) Explain application of ADC & DAC. 07
b) Design synchronous JK counter giving the following sequence 08