Total No. of Printed Pages:2

SUBJECT CODE NO:- E-354
FACULTY OF ENGINEERING AND TECHNOLOGY
S.E.(CSE/IT) (CGPA) Examination Nov/Dec 2017
Digital Electronics
(REVISED)

[Time: Three Hours] **[Max.Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 and Q.No.6 are compulsory.
ii) Solve any two questions from Q.2 to Q.5 and any two questions from Q.7 to Q.10.

Section – A

Q.1 **Solve any five questions.** 10

a) Represent the following number in one's complement form +8 and -8.

b) Design a 4 input NAND gate by using 2 input NAND gate only.

c) Convert following
i) $(25.57)_{10} = (?)_{BCD}$
ii) $(ABCDE)_{16} = (?)_{8}$

d) Perform following subtraction using 9's complement.
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e) State and prove De'morgans theorem.

f) What is mean by self complimenting codes?

g) Realize following expression using logic gates,
$Y = (A \oplus B).C + A\bar{B}C$

h) Reduce following using boolean algebra.
$Y = F(A,B,C) = \sum m(0,1,6,7)$

Q.2 a) What do you mean by weighted code? Explain BCD, Excess – 3 and gray code. 08

b) Reduce and realize following expression using NAND – NAND logic. 07
$F = \sum m(0,2,8,10,15) + \sum d(7,13)$

Q.3 a) Design a 4 bit adder with look ahead carry. 08

b) Draw and explain working of half and full subtractor along with its gates realization. 07

Q.4 a) Differentiate between analog and digital signals. 08

b) Design BCD to gray code converter. 07

Q.5 a) Given a logic equation below 08
i) Make a truth table
ii) Simplify using K map
iii) Realise using NAND gates only

$$f = ABC + B\bar{C}D + \bar{A}BC$$

b) Justify – NAND and NOR gates are called as universal gates. 07

Section – B

Q.6 **Solve any five.** 10

a) What is decoder? Explain with example.
b) Implement following equation using 4:1 multiplexer $y = \sum m(0,1,4,7)$ control i/p B & C.
c) What is parity encoder?
d) Draw logic symbol and truth table of J-K f/f.
e) What do you mean by race – around condition in J-K f/f.
f) Write types of shift registers.
g) Explain the advantages and disadvantages of synchronous counters.
h) Draw 4 bit SISO Right shift register.

Q.7 a) Design and implement circuit for 2 bit comparator using 4 line to 16 line decoder and multi input OR gate. 08

b) Draw NAND implementation of S-R f/f and explain its functionality with T.T. 07

Q.8 a) Design 1:16 demultiplexer by using two 1:8 demultiplexers and basic gates. 08

b) Explain working of 4 bit universal shift reg. 07

Q.9 a) Convert i) S-R f/f to T type f/f 08
ii) T type f/f to J-K f/f

b) Draw and explain the working of 4 bit asynchronous counter. 07

Q.10 a) What is PLD? Compare PROM. PLA and PAL. 08

b) Design 3 bit synchronous UP/DOWN counter using J-K f/f. 07