Total No. of Printed Pages:2

SUBJECT CODE NO:- P-501
FACULTY OF ENGINEERING AND TECHNOLOGY
S.E. (EEP/EE/EEE) Examination MAY/JUNE-2016
Analog & Digital Circuits
(Revised)

[Time: Three Hours] **[Max Marks:80]**

"Please check whether you have got the right question paper."

N.B i) Question number 1 and 6 are compulsory.
ii) Solve any two questions from remaining for each section.

Section A

Q.1 Solve any five of the following. 10
a) Define Load Line.
b) Draw symbol of Op Amp.
c) Define biasing BJT.
d) Define Slew rate of op amp.
e) Define voltage gain of BJT.
f) Draw Pin diagram of IC741.

Q.2 a) Explain ratings of BJT. 08
b) Explain Common base configuration of BJT. 07

Q.3 a) Explain Op-Amp parameter in detail. 08
b) Explain mono stable Multivibrator using IC555. 07

Q.4 a) An op amp has CMRR of 100dB. If its differential voltage gain is 40000 calculate common mode gain. 05
b) A certain transistor has $\alpha = 0.95$, ICO=$4\mu A$ and IB=$50\mu A$. Find the values of collector and emitter currents. 05
c) Explain Non-inverting Amplifier. 05

Q.5 Write a short note on any three. 15
a) Push Pull Amplifier
b) 78XX IC
c) First order low Pass Filter
d) FET Characteristics

Section B

Q.6 Solve any five from following. 10
a) $(1010111)_2 = (?)_{08}$
b) Find 1's compliment of $(110011001)_2$
c) Convert following from gray to binary. (1110110)
d) $(1010111)_2$- $(110011)_2$= ?
e) Explain NAND and NOR gate.
f) $(134)_{16} = (?)_{10}$

Q.7	a)	Construct AND, OR and NOT logic using NOR gate.	08
	b)	Explain the working of Demultiplexer.	07
Q.8	Simplify following equation using K Map.		15
	a)	$Y = BCD + A\bar{C}D + \bar{A}B\bar{C} + \bar{A}BD$	
	b)	$Y = A\bar{B}C + \bar{A}B\bar{C} + ABC$	
	c)	$Y = ABCD + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}D$	
Q.9	a)	Explain memory devices in detail.	08
	b)	Explain Shift Register.	07
Q.10	a)	Explain Synchronous Counter.	08
	b)	Explain edge triggered J K Flip-flop in detail.	07

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