Total No. of Printed Pages:2

SUBJECT CODE NO:- E-173
FACULTY OF ENGINEERING AND TECHNOLOGY
S.E.(EEP/EE/EEE) Examination Nov/Dec 2017
Analog & Digital Circuits
(OLD)

[Time: Three Hours] **[Max.Marks:80]**

Please check whether you have got the right question paper.

N.B
i. Q.NO.1 and Q.NO.6 are compulsory
ii. Attempt from each section any two questions from the remaining questions.
iii. Assume suitable data wherever necessary
iv. Figure to the right indicate full marks.

Section A

Q.1 Answer any five 10

A) Draw pin diagram of IC741
B) Draw symbol of PNP and NPN BJT.
C) What is zero-crossing detector?
D) Draw the input characteristics of common base mode and define its output resistance.
E) Mention some commonly used active filters.
F) Define Slew rate and CMRR of op amp.
G) Define biasing BJT.

Q.2 A) Compare CB, CC and CE configuration of BJT amplifier. 08

B) Derive the relation between α, β and γ. 07

Q.3 A) Draw and explain the circuit diagram of square wave generation using op-amp 07

B) Explain op-amp parameter in detail. 08

Q.4 A) Explain pin-diagram of IC555 with neat sketch. 07

B) With the neat diagram explain Instrumentation Amplifier and its application? 08

Q.5 Write short note on (Any three) 15

a) Push Pull Amplifier
b) 78XX IC
c) First order low pass filter
d) FET characteristics

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Section B

Q.6 Answer any five 10

A) Perform $(54)_{10} - (33)_{10}$ using 2's compliment?
B) Give the truth table and graphic symbol of D-flip-flop
C) Convert following from gray to binary (110110)
D) Convert hexadecimal no. AFC.25 into octal no. Define biasing BJT.
E) $(FA7)_{16}$ & $(1FD)_{16}$ Add no in binary form?
F) $(1029.55)_{10}$ Convert in to hex. No.
G) What are the advantages of dynamic RAM?

Q.7 A) Minimize the following using k-map 08
F(A,B,C,D,E)=$\prod$ M(6,9,11,13,14,17,20,25,28,29,30)

B) Explain race around condition in J-K flip flop? How can reduce it. 07

Q.8 A) Explain De-Morgan's theorem? 07

B) What are the advantages and disadvantages of dual slope ADC? Comment on their major applications 08

Q.9 A) Simplify following Boolean function in SOP form by K-map & draw logic dig. with AND-OR gate. F(A,B,C,D,E)= $\sum m(0,2,8,9,10,11,14,15)$ 07

B) Using NAND gate sketch clocked S-R flip-flop using this design master slave J-K flip-flop 08

Q.10 Write shorts note on (any three) 15

i. Semiconductor memories
ii. Characteristics of A to D converter
iii. Ring counter
iv. IC 555 mode of operation

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