Total No. of Printed Pages:7

SUBJECT CODE NO:- P-97

FACULTY OF ENGINEERING AND TECHNOLOGY

T.E.(EEP/EE/EEE) Examination May/June 2017

Microprocessor & Interfacing

(Revised)

[Time: Three Hours] **[Max.Marks:80]**

Please check whether you have got the right question paper.

N.B i) Q.No.1 and Q.No.6 are compulsory.
ii) Attempt any two questions from the remaining questions in each section
iii) assume suitable data & addresses if necessary
iv) Figure to the right indicates full marks.

Section A

Q.1	Solve any five		10
	1)	What is microprocessor?	
	2)	Explain function of instruction register	
	3)	Why program counter and stack pointer are 16 bit registers?	
	4)	What is opcode & operand	
	5)	How many T-states are required for opcode fetch & memory read operation	
	6)	What is function of $\overline{RD}$ & $\overline{WR}$ control signals	
	7)	Give functional categories of 8085 instructions	
	8)	What happens when STA C200H instruction executed	
Q.2	a)	Explain addressing modes of 8085	08
	b)	Draw the interrupt structure of 8085 and explain in brief	07
Q.3	a)	Draw and explain brief the flag register of 8085	08
	b)	Explain in detail CALL & RET instructions	07
Q.4	a)	Some numbers are stored from memory location D201H . Count of the number is stored at D200H. Write 8085 ALP to find largest number and store the result at C200 H . Handrun the program.	08
	b)	Explain in detail Architecture of 8085	07
Q.5	Write short notes on (Any three)		15
	1)	Stack and subroutines	
	2)	Concept of looping	
	3)	Features of Intel 8085	
	4)	Functions of SID & SOD pin	

2017

Section B

Q.6 Solve any five 10

1) What happens when following instructions are executed
   a) IN P_A b) OUT P_B
2) What is use of 8253 PIT
3) Enlist different I/O modes of 8255
4) Write O/P control word of 8255 in simple I/O mode all port O/P port
5) What is use of USART
6) Write output control signals used in 8259 A
7) Explain function of SID & SOD pin
8) What is ADC & DAC ?

Q.7
a) Explain in brief mode 0 and mode 1 of 8255 10
b) Write an 8085 ALP to output the data 22H, 33H , 44H, on port A, port B and Port C of 8255 respectively address of port A is 80H 05

Q.8
a) Explain block diagram of 8259 A 07
b) An 8253 is connected to 1 MH_Z clock it is used to generate a square signal of 1 Hz frequency give interfacing circuit & program to achieve 8085 based μp system assume address of counter O is 40H 08

Q.9
a) Explain the block diagram of 8279 08
b) Draw the interfacing diagram of stepper motor and write ALP to rotate in clockwise direction Assume delay subroutine is available at "DELAY" 07

Q.10 Write short notes (any three) 15

1) DC motor speed control
2) Measurement of frequency using 8085
3) Mode 0 of 8253
4) 8051 USART

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'Appendix A'

1. Programmable communication interface 8251 A :

(*i*) A synchronous mode format :

S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

(*ii*) Synchronous mode format :

SCS	ESD	EP	PEN	L_2	L_1	0	0

(*iii*) Command Instruction :

EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN

(*iv*) Status read :

DSR	SYN/ BRK	FE	OE	PE	TX EMPT	TX RDY	TX RDY

2. Programmable interval timer 8253 :

(*i*) Control work format :

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD

(*ii*) Mode reg. for latching count :

SC_1	SC_0	0	0	×	×	×	×

3. Programmable peripheral interface 8255 :

(*i*) Mode definition :

MSF	MS_2	MS_1	P_A	P_{CU}	MS	P_B	P_{CL}

P.T.O.

(*ii*) Bit set reset format :

BSR F	×	×	×	BS_2	BS_1	BS_0	BS/R

(*iii*) Mode 1-input status :

I/O	I/O A	IBF A	INTE A	INTR B	INTE B	IBF B	INTR B

(*iv*) Mode 1-output status :

OBF A	INTE A	I/O	I/O	INTR A	INTE B	OBF B	INTR B

(*v*) Mode 2 status :

OBF A	INTE 1	IBF A	INTE 2	INTR A	×	×	×

Programmable DMA controller 8257 :

(*i*) Mode set register :

EAL	ETCS	EEW	ERP	ECH3	ECH2	ECH1	ECH0

(*ii*) Count register :

R/W/V 1	RWV 0	D_{13}	D_{12}	....	....	D_1	D_0

(*iii*) Status register :

0	0	0	UF	TCS_3	TCS_2	TCS_1	TCS_0

5. Programmable interrupt controller 8259 :

(i) ICW_1 :

A_7	A_6	A_5	1	LT1	AD1	SMG1	ICW 1

(ii) ICW_2 :

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

(iii) ICW_3 (Slave) :

0	0	0	0	0	ID_2	ID_1	ID_0

(iv) ICW_3 (Master) :

S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

(v) ICW_4 :

0	0	0	SFN	BUF	M/S	AEO_1	MPM

(vi) OCW_1 :

M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

(vii) OCW_2 :

R	SL	EOI	0	0	L_2	L_1	L_0

(viii) OCW_3 :

0	ESM M	SMM	0	1	P	RR	RIS

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2017

mable KBD/Display controller 8279 :

D/Display Mode Set :

0	0	0	D	D	K	K	K

(*ii*) Program clock :

0	0	1	P	P	P	P	P

(*iii*) Read FIFO/Sensor RAM :

0	1	0	A_1	×	A	A	A

(*iv*) Read Display RAM :

0	1	1	A_1	A	A	A	A

(*v*) Write Display RAM :

1	0	0	A_1	A	A	A	A

(*vi*) Display write Inhibit/Blanking :

1	0	1	×	IW A	IW B	BL A	BL B

(*vii*) Clear :

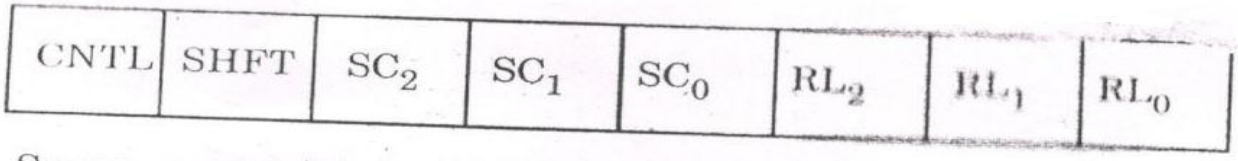
1	1	0	C_D	C_D	C_D	C_F	C_A

(*viii*) End Interrupt/Error mode set :

1	1	1	E	×	×	×	×

2017

(ix) Scanned KBD data format for key code :



(x) Sensor matrix data format for key code (switch) :