[Total No. of Printed Pages:4] **CODE NO:- Z-134**

FACULTY OF ENGINEERING

T.E (EEP/EE/EEE) - Year Examination June– 2015

Microprocessor and Interfacing

(Revised)

[Time: Three *Hours*] **[Max. Marks: 80]**

"Please check whether you have got the right question paper."

i) Question No.1and Question No 6 are compulsory
ii) Attempt any two questions from remaining questions from each section.
iii) Assume suitable data if necessary

SECTION A

Q.1 Solve any five 10

a) List various instructions that can be used to clear accumulator in 8085
b) What is need of ALE signal in 8085
c) Why multiplexing is done in 8085
d) What is DMA
e) Why address bus is unidirectional
f) What is function of NOP instruction
g) Define machine cycle
h) What are flags?

Q.2 a) Draw internal architecture of 8085 microprocessor and explain function of each block in brief 08
b) Enlist data transfer instructions of 8085 & explain any four in detail 07

Q.3 a) Write a program to add ten data bytes. Data is stored in memory location starting from C200H. The result is 8 bit only. store the result at C300H location 08
b) What are subroutines? Explain (ALL & RET instructions) 07

Q.4 a) Explain addressing modes of 8085 08
b) Explain SIM & RIM instructions of 8085 07

Q.5 Write short notes on (any three) 15

1) Flag register of 8085
2) Measurement of frequency using 8085
3) MP based protective Relays
4) Interrupts of 8085

SECTION B

Q.6 Solve any five 10

a) What is purpose of 8255 PPI?
b) Define instruction cycle
c) Explain DAA instruction
d) Explain XCH_4instruction
e) What happens when IN instruction executed
f) What is difference in ADC & DAC?
g) What is function of interrupt request register in 8259?
h) What is I/O map I/O mode

Q.7 a) Draw the interfacing diagram to interface 8 LED's to 8085 thro[1] port A & port B of 8255 & write ALP such than when P_ALED's are ON P_B LED's are OFF and vice versa 08

b) Explain block diagram of 8253 PIT 07

Q.8 a) An 8253 is connected to 1MHZ clock, it is used to generate a square signal of 1 KH_Z. frequency. Give the interfacing circuit & the program to achieve in an 8085 based up system. Assume the addresses of counters & control register as 40H, 41H, 42H & 43H respectively 08

b) Draw the interfacing diagram of stepper motor with 8085 using 8255. Write ALP to rotate it in clockwise direction. Assume delay subroutine is available at "DELAY" 07

Q.9 a) Explain in detail cascaded PIC system of 8259 07

b) Explain block diagram of 8279 in detail 08

Q.10 Solve <u>any three</u> 15

1. Specifications of ADC & DAC
2. Block diagram of 8255
3. 8251 USART
4. DC motor speed control

'Appendix A'

1. Programmable communication interface 8251 A:
   i) A synchronous mode format :

S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

   ii) synchronous mode format :

SCS	ESD	EP	PEN	L_2	L_1	0	0

   iii) command instruction :

EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN

   iv) status read :

DSR	SYN/ BRK	FE	OE	PE	TX EMPT	TX RDY	TX RDY

2. Programmable interval timer 8253 :
   i) Control work format :

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD

   ii) Mode reg. for latching count :

SC_1	SC_0	0	0	x	x	x	x

3. Programmable peripheral interface 8255 :

i) Mode definition :

MSF	MS_2	MS_1	P_A	P_{CU}	MS	P_B	P_{CL}

ii) Bit set reset format :

BSR F	x	x	x	BS_2	BS_1	BS_0	BS/R

iii) Mode 1 – input status :

I/O	I/O A	IBF A	INTE A	INTR B	INTE B	IBF B	INTR B

iv) Mode 1 – output status :

OBF A	INTE A	I/O	I/O	INTR A	INTE B	OBF B	INTR B

v) Mode 2 status :

OBF A	INTE A	IBF A	INTE 2	INTR A	x	x	x

4. Programmable DMA controller 8257 :

i) Mode set register :

EAL	ETCS	EEW	ERP	ECH3	ECH2	ECH1	ECH0

ii) Count register :

R/W/V 1	RWV 0	D_{13}	D_{12}	….	….	D_1	D_0

iii) status register :

0	0	0	UF	TCS_3	TCS_2	TCS_1	TCS_0

5. Programmable interrupt controller 8259 :

i) ICW_1 :

A_2	A_6	A_5	1	LT1	AD1	BMG_2	ICW4

ii) ICW_2 :

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_0	A_0

iii) ICW_8(Slave) :

0	0	0	0	0	ID_2	ID_1	ID_0

iv) ICW_3 (Master) :

S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

v) ICW_4 :

0	0	0	SFN	BUF	M/S	AEO_1	MPM

vi) OCW_1 :

M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

vii) OCW_2:

R	SL	EOI	0	0	L_2	L_1	L_0

viii) OCW_3:

0	ESMM	SMM	0	1	P	RR	RIS

6. Programmable KBD/Display controller 8279 :

i) KBD/Display mode set :

0	0	0	D	D	K	K	K

ii) program clock :

0	0	1	P	P	P	P	P

iii) read FIFO/Sensor RAM :

0	1	0	A_1	X	A	A	A

iv) Read Display RAM :

0	1	1	A_1	A	A	A	A

v) Write Display RAM :

1	0	0	A_1	A	A	A	A

vi) Display write inhibit/Blanking :

1	0	1	X	IWA	IWB	BLA	BLB

vii) Clear :

1	1	0	C_D	C_D	C_D	C_F	C_A

viii) End Interrupt/Error mode set :

1	1	1	E	x	x	x	x

ix) Scanned KBD data format for key code :

CNTL	SHFT	SC_2	SC_1	SC_0	RL_2	RL_1	RL_0

x) Sensor matrix data format for key code (switch) :

RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0